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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,011	07/11/2003	Chien-Ping Huang	59552 (71987)	4390
7590	07/07/2004		EXAMINER	
Mr. Peter F. Corless EDWARDS & ANGELL, LLP 101 Federal Street Boston, MA 02110				CLARK, JASMINE JHIHAN B
		ART UNIT	PAPER NUMBER	2815

DATE MAILED: 07/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,011	HUANG, CHIEN-PING	

-- The MAILING DATE of this communication appars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 14 June 2004.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-20 is/are pending in the application.
 4a) Of the above claim(s) 1-8 is/are withdrawn from consideration.
 5) Claim(s) 17-20 is/are allowed.
 6) Claim(s) 9 and 12 is/are rejected.
 7) Claim(s) 10, 11 and 13-16 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date 07/11/03.

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

Election

1. Claims 1-8 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group I, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/14/04.
2. It is suggested that Applicant cancels claims 1-8 in response to this Office action.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claims 9 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (US 6,528,722 B2).

Huang teaches a Ball Grid Array (BGA) semiconductor package (see Fig. 7 eg.,), comprising a core layer (52) having a first surface and an opposite second surface, and a through hole penetrating through the core layer, wherein the second surface is formed with a plurality of wire bonding portions around the through hole, a plurality of ball-bonding portions; and a plurality of intended-exposing regions around the wire bonding portions; at least one chip (53) mounted on the first surface of the core layer 52 and over the through hole, with a portion of the chip exposed via the through hole; a solder mask layer (51) (see column 4, lines 66-67) applied over the second surface of the core layer (52) with the ball-bonding portions being exposed, wherein the solder mask layer (51) is formed with an opening for exposing the through hole, the wire-bonding portions (54), and the intended-exposing regions; a plurality of bonding wires (54) which penetrate through the through hole and electrically connect the chip (53) to the bonding-wire portions; a first encapsulation body formed on the first surface of the core layer (52) for encapsulating the chip (53); a second encapsulation body formed on the second surface of the core layer for encapsulating the bonding wire and the intended-exposing regions; and a plurality of solder balls (56) deposited on the ball-bonding portions. Note that there is no structure claimed in these claims which could distinguish them over the prior art shown in Fig. 7.

Allowable Subject Matter

Art Unit: 2815

4. Claims 10, 11, 13-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The applied reference fails to teach and/or suggest as follows:

- wherein a width of the intended-exposing region is of a range from 0.4 to 0.8 mm and/or 0.4 mm as claimed in claims 10 and 11.
- wherein the opening of the solder mask layer is larger in width than a mold cavity of a mold used for forming the second encapsulation body as claimed in claim 13.
- wherein a thickness of the second encapsulation body covering the intended-exposing regions is substantially equal to that of the solder mask layer as claimed in claim 14.
- comprising a layer of patterned conductive traces that applied between the second surface of the core layer and the solder mask layer as claimed in claim 15; and another solder mask layer that applied between the first surface of the core layer and the chip as claimed in claim 16.

5. Claims 17-20 are allowed.

The following is an examiner's statement of reasons for allowance: as per the above discussion the applied reference fails to teach and/or suggest having a conductive trace layer that applied over the second surface of the core layer, and formed with a plurality of wire-bonding portions around the through hole, a plurality of

ball-bonding portions, and a plurality of intended exposing regions around the wire bonding portions; and a solder mask layer that applied over the conductive traces layer with the ball bonding portions being exposed, and formed with an opening for exposing the through hole, the wire bonding portions, and the intended-exposing regions.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

References Cited

6. Bai (US 2004/0061239 A1), Sasaki (US 6,661,099 B2), Jiang et al. (US 2002/0100989 A1), and Chia-Yu et al. (US 6,385,049 B1) show a similar structure to Huang et al. (US 6,528,722 B2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine J Clark whose telephone number is (571) 272-1726. The examiner can normally be reached on Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jjbc/07/06/04

**JASMINE CLARK
PRIMARY EXAMINER**

